A New Time Domain-Based Busbar Protection Algorithm

F. A. M. Vásquez, E. P. Ribeiro, K. M. Silva, F. V. Lopes

***Abstract*—This paper presents a new time domain busbar protection algorithm which uses current samples and their half-cycle incremental quantities to implement a fast and reliable tripping logic. The sign of incremental quantities is used to determine the fault direction and to distinguish internal from external busbar faults. Also, a differential incremental current is calculated for properly selecting the circuit breakers that must be opened to clear the fault. In order to test the proposed technique, a double-bus single-breaker busbar configuration was modeled in ATP/ATPDraw software and several types of internal, external and evolving faults are simulated. The results reveal the proposed function quickly operates for internal faults and ensures security for external faults. Moreover, the proposed approach allows a fast detection of internal faults during an external fault. Hence, although the proposed function is based on well-known fundamentals, it achieves the principal requirements for a busbar protection scheme with a high degree of adaptability and reliability for severe cases.**

***Keywords*—Busbar, Differential Protection, Directional Protection, Incremental quantities, ATPDraw.**

I. Introduction

THE busbars are the more critical elements of power systems because a fault within its protection zone causes the disconnection of all connected circuits, which may lead to stability issues and, consequently, to widespread blackouts. Thus, the protection system must be fast to eliminate internal faults and secure for external faults, even when the current transformer (CT) saturates. Additionally, the algorithm must track the configuration of dynamic arrangements, guaranteeing selectivity and dependability [1]. To do so, busbar protection algorithms are usually based on the traditional differential and directional principles [2]. Differential elements use operation and restraint signals, requiring a protection zone logic for correct calculations [3]. Conversely, the directional principle checks the polarity of currents, being used to supervise the differential element in some commercially available relays [4].

The traditional differential protection is based on current signals and it is well explained in [5]. This algorithm uses the well-known tripping logics 1-out-of-1 and 2-out-of-2, formulated for internal and evolving faults, respectively. This function can provide a mean operation time of a quarter-cycle, but the presence of the decaying DC component can delay it. An alternative partial differential current approach was proposed by [6], but high fault resistances and evolving faults represent serious issues. In turn, [7] used a generalized alpha plane approach, but it presents instabilities during transient period after fault inception, then an improved alpha plane-based function was developed by [8]. Recently, [5] proposed an instantaneous-power-based differential scheme with reduced time operation, but it experiences problems if the DC component is not correctly filtered. Also, the Park's transformation applied on current signals was used by [9], leading to reduced time response, but it can not be applied to monopolar circuit breaker operation. There are also some proposals that use the wavelet transform approach, [10]–[13], but they need a high sampling frequency and they may present difficulty for dealing with evolving faults. In contrast, transient-based methods [14], [15] provide a very fast response but damped transients represent a challenge for these techniques. In addition, the machine learning-based algorithms [16], [17], [18] provide high accuracy, but numerous computer simulations need to be carried out for this purpose.

With another approach, [19] developed an incremental directional signal with fast operation but its performance can be jeopardized in case of severe CT saturation. Also, [20] applies a phase-mode transformation on current signals to obtain an incremental signal, but the window used to calculate it represents a delay for its operation. As well as differential techniques, [21] also used the wavelet transform approach to provide very fast fault clearance. In this category, [22] proposed to use the polarity and magnitude of the signals resulting from the application of the same transformation on currents. In the same category, [23] developed a decision-making unit from morphological gradient applied on the superimposed currents. However, the potential of this algorithm was not proved for severe external faults.

In this context, this paper proposes a time-domain busbar protection technique based on the calculation of incremental currents in a half-cycle window. With this approach, the developed protection function combines the traditional differential and directional principles. Here, the direction of incremental signals discriminates an internal fault from an external fault and the polarity of the differential current is used for identifying a faulted bus. Then, the proposed algorithm needs to know the states of auxiliary contacts of switch disconnectors and circuit breakers to define the circuits that must be disconnected in case of an internal fault, but it does not need a protection zones logic.

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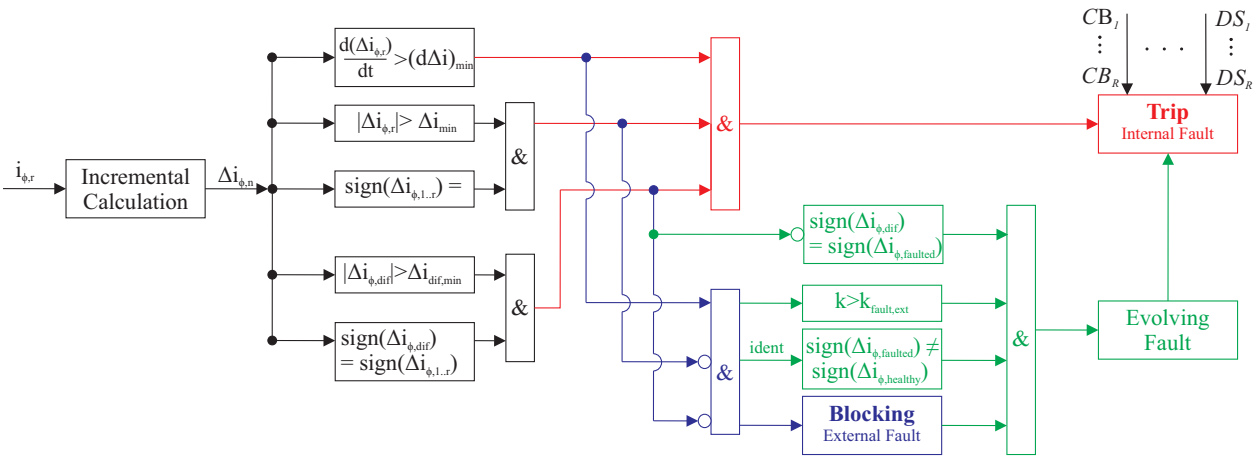

Fig. 1: Operation logic of the proposed algorithm

II. Proposed Algorithm

The proposed operation logic aims to provide a fast response for internal faults, security in case of external faults and sensitivity for recognizing the evolution of an external fault to an internal fault, even in cases of CT saturation. In this sense, the currents measured by CTs initially pass through an anti-aliasing filter and discretized with 64 samples per cycle. After that, the proposed function requires the normalization of these signals in order to compensate mismatches in CT ratios, as taken into account in modern relays [4]. The normalization begins with the determination of the factor $TAP_{\phi,r}$, for each phase, ϕ, for each bay, r, through

$$TAP_{\phi,r} = \frac{CTR_{MAX} I_{NOM}}{CTR_r}, \tag{1}$$

where CTR_{MAX} and I_{NOM} are respectively the largest ratio among the installed CTs and its nominal secondary current, and CTR_r is the CT ratio of the corresponding terminal. From that, the discretized current signals, $i'_{\varphi,r}$, are divided by $TAP_{i,r}$, resulting to the normalized per unit current signals, $i_{\varphi,r}$. Hereafter, the incremental currents, $\Delta i_{\phi,r}$, considering half-cycle approach, are calculated as:

$$\Delta i_{\phi,r}(k) \quad = \quad i_{\phi,r}(k) + i_{\phi,r}(k - N/2). \tag{2}$$

This per phase calculation for each bay is the base for the protection logic, illustrated in Fig. 1. This algorithm initially needs a disturbance detection which is performed by the derivative of incremental quantities:

$$der(\Delta i_{\phi,r}(k)) \quad = \quad \frac{\Delta i_{\phi,r}(k) - \Delta i_{\phi,r}(k-1)}{dt}, \tag{3}$$

where dt is the sampling period. Also, the differential incremental current is calculated as:

$$\Delta i_{\phi,dif}(k) = \sum_{r=1}^{R} \Delta i_{\phi,r}(k). \tag{4}$$

where R represents the total number of circuits connected to busbar without considering the separation of logic protection zones depending on the topology. Differently of traditional

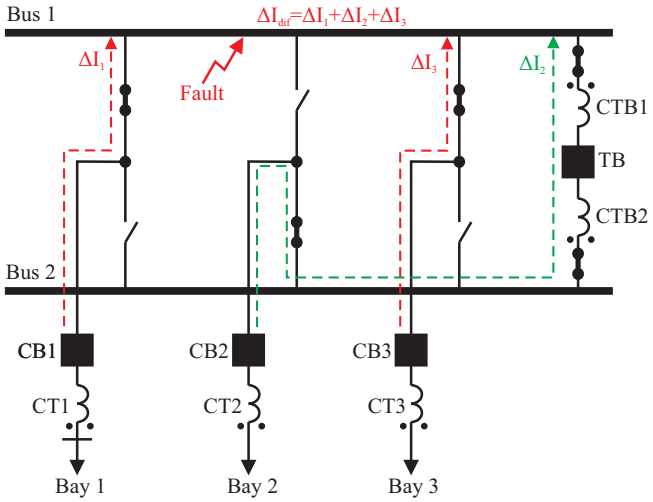

Fig. 2: Directionality of $\Delta i_{\phi,r}$ for an internal fault.

elements, which uses a protection zone logic [2] to calculate the differential current, the proposed technique uses it only as a final step for determining the bus where each bay were initially connected, but not for differential signal calculation. From that, the logic for internal, external and evolving faults can be implemented.

1) Internal Faults: the first condition for recognizing an internal fault is the detection of a disturbance. For that, the derivative of the incremental current on the faulted phase must be higher than a minimum threshold, i.e., $d(\Delta i_{\phi,r})/dt > (d\Delta i)_{min}$. After the disturbance is detected, it must be verified that the absolute values of incremental currents, per phase ϕ of bays, r, are higher than a minimum value, i.e., $|\Delta i_{\phi,r}| > \Delta i_{min}$. At the same time, as shown in Fig. 2, an internal fault causes the current contributions to flow into the bus. Thus, the incremental currents of connected circuits have the same polarity, i.e., "$sign(\Delta i_{\phi,1..r})$ =". On the other hand, the incremental quantity of the differential current per phase, $\Delta i_{\phi,dif}$, calculated from current contributions must be also higher than a minimum threshold, i.e., $|\Delta i_{\phi,dif}| > \Delta i_{dif,min}$. Finally, the polarity of $\Delta i_{\phi,dif}$, must be the same of the

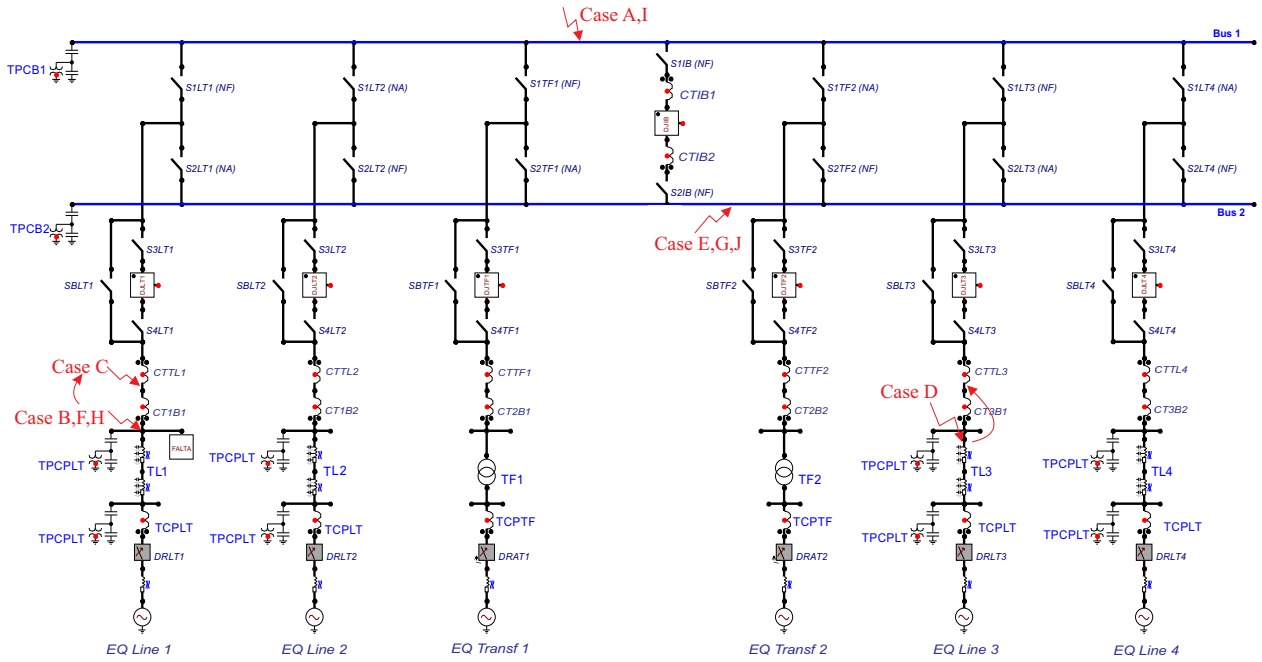

Fig. 3: Simulated power system.

individual incremental currents of connected circuits, i.e., $sign(\Delta i_{\phi,dif}) = sign(\Delta i_{\phi,1..r})$. If the described conditions are satisfied, the proposed protection function recognizes the fault within the busbar protection zone.

Now, the Fig. 2 helps to understand how to correctly choose the circuit breaker to be opened based on the incremental currents. It can be observed that bays 1 and 3 are connected to Bus 1, and bay 2 is connected to Bus 2, through switch disconnectors. It can be observed that when a fault occurs in the bus zone, the currents measured by the current transformers, CT1, CT2 and CT3, will have an initial positive sign since they enter the busbar. Also, the current I_2, flows from Bus 2 to Bus 1, i.e., the polarity of the current measured by CTB2 is also positive, and it is the same current flowing into CTB1 with opposite polarity. By extending this analysis to the incremental quantities, without loss of generality, in this situation, the polarity of $\Delta I_{dif} = \Delta I_1 + \Delta I_2 + \Delta I_3$, and the polarity of the incremental current calculated from CTB2 measurement is the same. If these conditions happen, it is confirmed that the fault occurred at Bus 1, so all circuit breakers connected to it must be opened, i.e. CB1 and CB3, as well as the tie breaker, TB. Analogously, if the polarity of ΔI_{dif} is equal to the polarity of the incremental current calculated from CTB1, all bays connected to Bus 2, and the tie breaker, must be opened. The selectivity of the function is then guaranteed by knowing the status of circuit breakers and disconnect switches once all feeders connected to a faulted busbar must be disconnected.

2) External Faults: if the fault occurs outside the busbar protection zone, the disturbance detector is also sensitized. Also, the incremental quantities of individual currents can achieve values higher than the minimum threshold. The corresponding minimum limit of the incremental differential current can also be exceeded in case the CT of the faulted bay saturates. However, the other conditions are not satisfied. It means that the incremental current of the faulted bay has an opposite polarity in relation to the healthy feeders, i.e., $sign(\Delta i_{\phi,faulted}) \neq sign(\Delta i_{\phi}, healthy)$. Also, the incremental differential current after CT saturating has the same polarity of the healthy feeders and it is opposite to the faulted bay. If these conditions are satisfied, the function recognizes an external fault at instant $k_{fault,ext}$ and the operation is blocked.

3) Evolving Faults: although the tripping signal can be correctly inhibited for an external fault, it is necessary to provide adaptability for the protective function in case the short-circuit evolves into the busbar protection zone. For this purpose, the protection function continues to monitor the current signals after an external fault detection, i.e., $k > k_{fault,ext}$, aiming to unblock the tripping command when the evolution takes place. This additional logic for evolving faults firstly checks if the flag of relay inhibition is active. Also, for the sake of security, the logic redundantly verifies if there is a current with opposite polarity in relation to the rest, i.e. $sign(\Delta i_{\phi,faulted}) \neq sign(\Delta i_{\phi}, healthy)$. As previously explained, that occurs in case of an external fault. When the external fault finally evolves to an internal fault, the incremental differential current and the incremental current of the bay, where external fault occurred, acquire the same polarity, i.e., $sign(\Delta i_{\phi,dif}) = sign(\Delta i_{\phi,faulted})$. Nevertheless, the polarity of the other current contributions is not the same as $\Delta i_{\phi,dif}$ before the evolution. Then, the input of this block is the comparison of $\Delta i_{\phi,dif}$ with all individual incremental currents, but once this condition is not fully satisfied, it is initially negated, as shown in the logic diagram. If these conditions are satisfied, the evolution of the fault is recognized, the logic value of the external fault flag becomes zero, so the relay is unlocked to send the trip command to the circuit breakers.

III. Results and Discussion

The proposed algorithm is tested by using a 230 kV/60 Hz power system, modeled in ATP/ATPDraw and shown in Fig. 3. It consists of a substation with the double-bus, single-breaker configuration, which is characterized by its high degree of flexibility. With this topology, the two buses are always energized and they are interconnected through the tie breaker. It is composed of four bays with transmission lines (TL), and two bays with power transformers (TF). The circuits TL1, TF1, and TL3 are initially connected to Bus 1, and the other circuits are connected to Bus 2. The parameters of transmission lines, power transformers TF1, and Thevenin power system equivalents are detailed in [13]. The signals obtained from CTs were obtained with a time-step of 1 μs. A low-pass anti-aliasing Butterworth filter was then used to eliminate high-frequency components. After that, the signals were sampled using the sampling frequency f_s=3840 Hz, corresponding to 64 samples per cycle in a 60 Hz power system. The model of CTs is reported in appendix B.3 of [24]. In order to visualize the response time of the proposed technique, the flags of the disturbance detector, internal fault and external faults, are respectively represented by *FDD*, *FINT* and *FEXT*.

A. Internal fault in Bus 1

In this case, a phase A to ground (AG) fault occurs at 101.8 ms at Bus 1, which represents a fault at 90^o of the voltage signal. It can be observed in Fig. 4 that, immediately after the fault inception, all incremental currents increase with positive polarity. Also, the differential incremental current increases with the same polarity, and it can be noticed that its amplitude is higher than individual contributions. As a result, the disturbance is detected in 103.4 ms, and the internal fault is identified at 103.6 ms, i.e. less than 2 ms after fault inception. From this instant, the trip command must be sent to the correct circuit breakers. Therefore, Fig. 5 reveals that, immediately after fault inception, the polarity of the incremental current of the CT installed on the coupler circuit, on the Bus 2 side, Δi_{TC1B2} and Δi_{dif} are positive, i.e. there is a contribution coming from Bus 2 to Bus 1, then it confirms the fault in Bus 1. In order to compare the proposed function with a conventional busbar protection scheme, the time-domain current-based differential protection described by [5] was also implemented with a sampling frequency of 64 samples per cycle. Its response is shown through the differential current, i_{op}, and the restraint current, i_{res}, multiplied by an slope, *SLP*, and its operation of this algorithm depends on the time i_{op} is higher than $i_{res}*SLP$. As shown in Fig. 6, this function allows to recognize the fault at 107,01 ms through its fast operation logic 1-out-of-1, and the backup logic 2-out-of-2 could operate at 112,49 ms. Then, the incremental current-based function demonstrates to be pretty faster than the traditional approach.

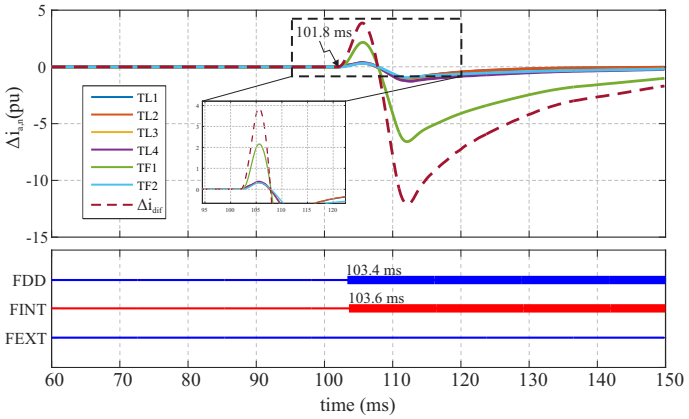

Fig. 4: Case A. Internal fault in Bus 1 at 101.8 ms.

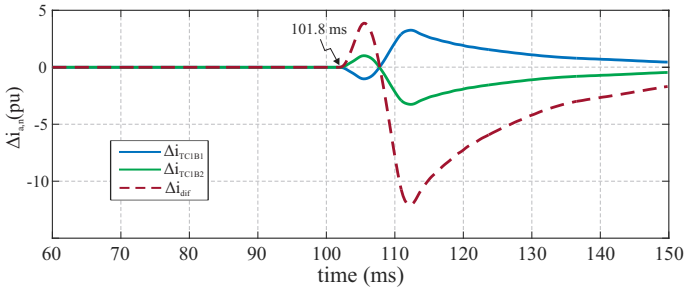

Fig. 5: Case A. Comparison of incremental currents of CTs installed on tie circuit and Δi_{DIF}.

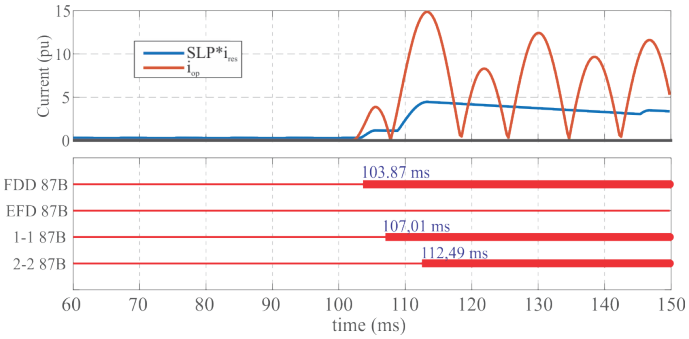

Fig. 6: Case A. Response of traditional current-based differential protection. Internal fault in Bus 1 at 101.8 ms.

B. External fault with CT saturation

In this case, the simulation consists of applying an AG external fault at 72.30 ms in the bay of the first transmission line, TL1. This fault causes the saturation of the corresponding CT, leading to a severe distortion of the current waveform, i_a, of bay TL1, as seen in Fig. 7. Also, it can be seen that, immediately after the fault instant, $\Delta i_{a,TL1}$ increases with positive polarity and contrary to all the others incremental currents. Also, it is possible to see that Δi_{dif} remains close to zero during an interval after the fault until CT saturation takes place. When it happens, Δi_{dif} acquires values with opposite polarity in relation to the incremental current of the faulted bay, and this polarity never changes. In these conditions, the external fault is recognized and no trip command is never issued.

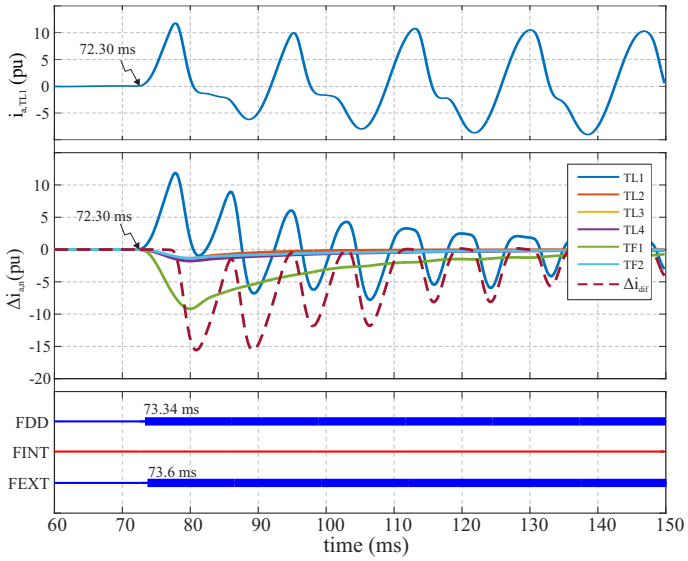

Fig. 7: Case B. External fault on bay of transmission line, TL1.

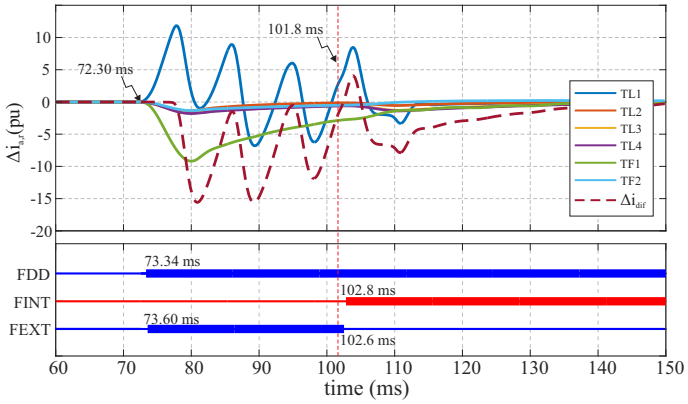

Fig. 8: Case C. Evolving fault from external AG fault to internal ABG fault (Phase A).

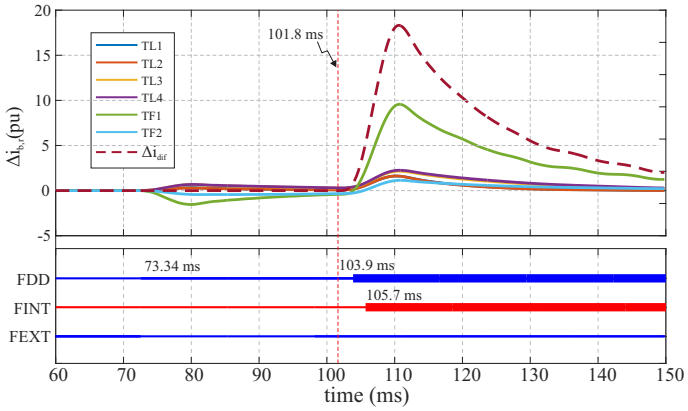

Fig. 9: Case C. Evolving fault from external AG fault to internal ABG fault (Phase B).

C. Evolving External-to-Internal Fault with CT saturation

In this case, the same external fault of Section III-B is simulated and an internal fault, ABG, takes place at 101,8 ms, as illustrated in Fig. 3. Also, both external and internal fault occurs without ground resistance or phase-to-phase resistance. As shown in Fig. 8, the external fault is detected at 73.60 ms. The first step to identify the eventual evolution of the fault is the tripping blocking command itself and monitor the signal after this instant. Before the evolution, the algorithm continues to see that there is an incremental current, $\Delta i_{a,TL1}$, with polarity opposite to the rest. Also, the comparison of $\Delta i_{dif,a}$ with individual contributions in phase A, $\Delta i_{a,r}$, in this scenario, leads to dispose of an internal fault case, and while evolution does not occur, the polarity of $\Delta i_{dif,a}$ never will be change. Nevertheless, when the internal fault takes place at 101,8 ms, the polarity of $\Delta i_{a,dif}$ change so it acquires the same polarity of the initially faulted signal, $\Delta i_{a,TL1}$, so the internal fault is recognized at 102,8 ms. On the other hand, it is possible to see in Fig. 9 that the disturbance is detected in phase B only at 103,9 ms, and the internal fault is confirmed at 105,7 ms. The operation delay of this phase element is caused by the time for all $\Delta i_{b,r}$ increasing and getting the same polarity due to this adverse scenario.

D. Evolving External-to-Internal Fault without CT saturation

In this case, a phase-to-ground AG short-circuit is applied on the bay LT3 at 75 ms and it evolves into the busbar protection zone at 82 ms, i.e., the internal AG fault appears less than half cycle from the occurrence of the external fault. This evolution occurs without CT saturation. According to Fig. 10, the external fault is detected at 76.21 ms, after the polarity of fault incremental current becoming opposite to the others signals. Once there is no CT saturation associated with the external fault, the incremental differential current, Δi_{dif}, remains close to zero. This signal only increases after the internal fault takes place, acquiring the same polarity of the initial faulted signal, Δi_{TL3}. Thus, the external fault flag, FEXT, is deactivated and the internal fault is recognized at 84,83 ms.

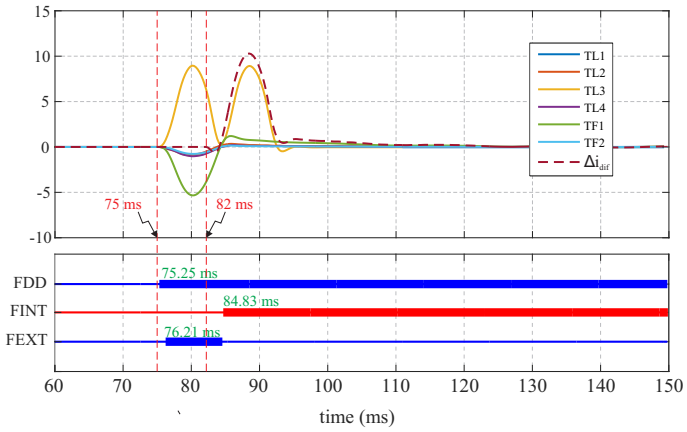

Fig. 10: Case D. Evolving external-to-internal fault without CT saturation in phase A.

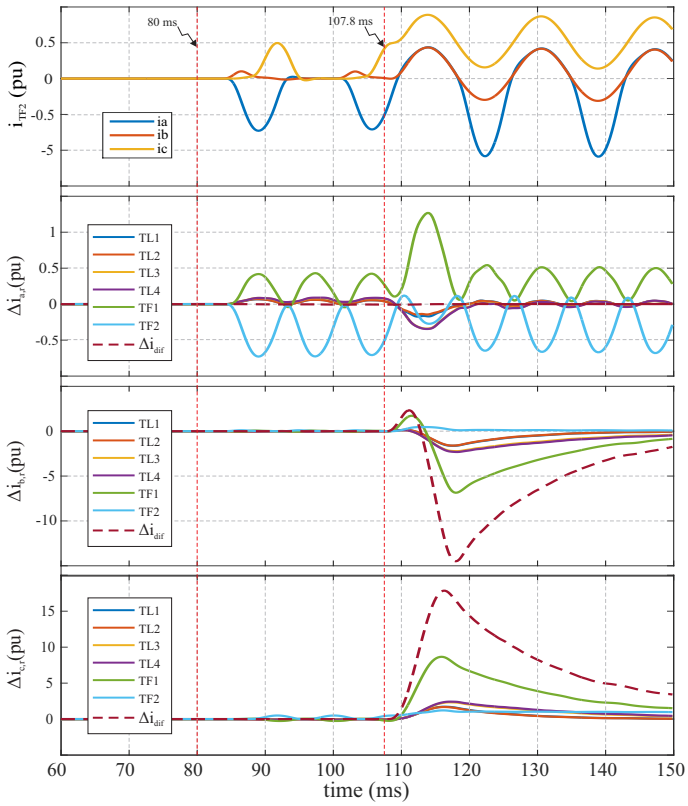

Fig. 11: Case E. $i_{\phi,TF2}$ and $\Delta i_{\phi,r}$.

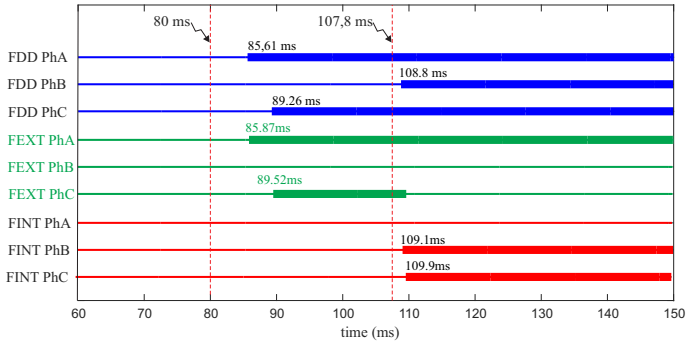

Fig. 12: Case E. Operation flags.

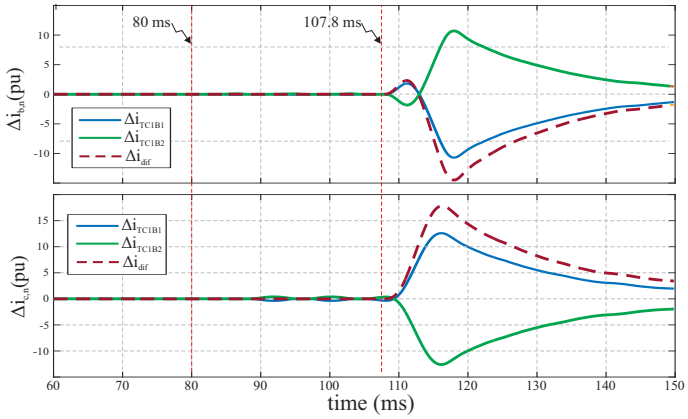

Fig. 13: Case F. Polarity comparison for circuit breaker selection for a fault in the coupler circuit.

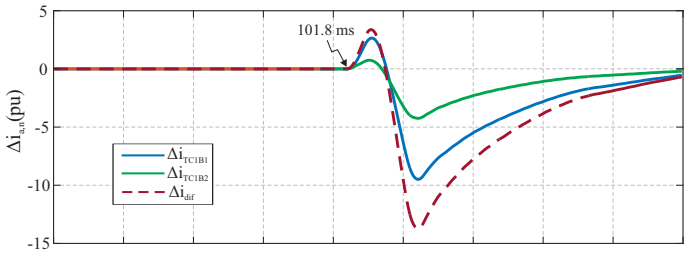

Fig. 14: Case E: Internal AT fault in the coupler circuit.

E. Internal Fault During a Transformer Energization

In this case, the energization of the transformer, TF2, is simulated by connecting it to Bus 2 at 80 ms. After that, an internal two-phase-to-ground fault, BCG, is applied on this bus at 107,8 ms. The current waveforms of TF2 are firstly presented in Fig. 11. In this figure, it can also be noted that the energization leads to having non zero values of $\Delta i_{a,r}$ and $\Delta i_{c,r}$ from the instant where each phase current is distorted. Nevertheless, $\Delta i_{a,dif}$ remains zero so that even if the disturbance is detected, the severity of the event only can lead to classify the event as an external fault. In turn, the disturbance in phase B is detected just at fault instant, then the internal fault is recognized at 109.1 ms, as shown in Fig. 12. In relation to phase C, the disturbance is detected from the energization, and its severity leads to identify an external fault. However, when the internal fault happens, the algorithm recognizes it at 109.9 ms. Finally, in Fig. 13, it can be noted that $\Delta i_{a,dif}$ and $\Delta i_{b,dif}$ have the same polarity of $\Delta i_{a,TC1B1}$ and $\Delta i_{b,TC1B1}$, respectively, so it can be confirmed that the fault occurred on Bus 2.

F. Internal fault in Coupler Circuit

In this case, the fault occurs between the CTs installed in the coupler circuit, where all bays represents a contribution for the short-circuit. It can be seen if Fig. 14 that the polarity of incremental currents of both CTs, *TC1B1* and *TC1B2*, installed in this circuit is the same of Δi_{dif}. That means that there is a contribution coming from Bus 1, as well as from Bus 2. In this case, all circuit breakers must be opened.

G. Internal Fault with Fault Resistance

The objective of this study is to test the sensitivity of the algorithm for faults with different degrees of fault resistance. In this case, the resistances of an internal fault, AG, at 101.8 ms on Bus 2, considered for these simulations were 0 Ω, 100 Ω, 200 Ω and 300 Ω. Fig. 15 reveals that the technique experiences a delay as long as the fault resistance increases. However, for 300 Ω, the decision time is only 1.1 ms longer than in the solid fault case. Then, it can be noticed that this factor does not critically impact on the performance of the proposed function.

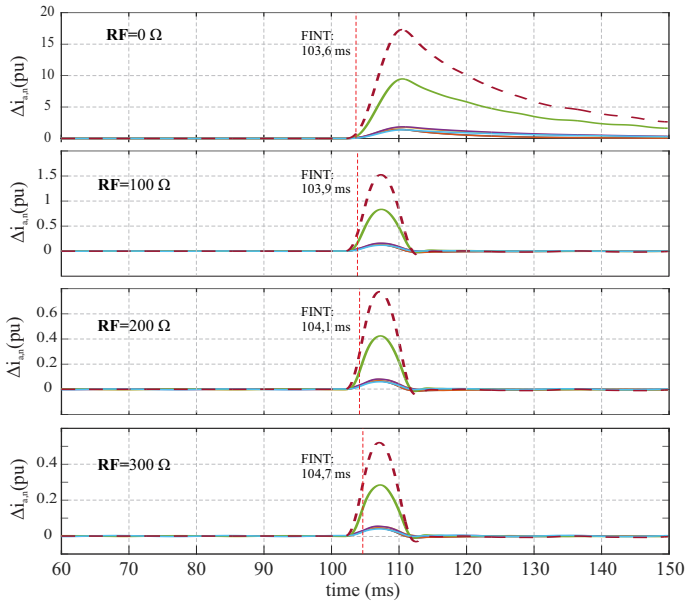

Fig. 15: Case G: Internal AT fault for different fault resistances.

H. Comparison with One-Cycle Incremental Quantities

In this case, the same external fault with CT saturation of Section III-B is also applied, but the incremental signals are calculated using a one-cycle interval between samples. As demonstrated in this previous section, the half-cycle incremental differential current approach acquires values different from zero after the CT saturates and it keeps the same polarity after this instant. Contrarily, if the one-cycle approach is used, the differential current can experience a change of polarity, so it acquires the same polarity of the incremental phase current where the external fault had occurred, as shown in Fig. 16. This scenario erroneously fits in an evolving fault case and the relay wrongly recognizes an internal fault at 95,53 ms. In view of that, the one-cycle approach may not continuously help to suitably indicate the polarity of a severe external fault due to the CT saturation. On the contrary, this is not a drawback for the half-cycle approach so the proposed technique is robust and immune for severe CT saturation scenarios.

I. Impact of Sampling Frequency

In order to evaluate the impact of sampling frequency on the proposed method, an internal fault, BG, is applied on Bus 1 at 90 ms and the sampling frequencies of 16, 32, 64, and 128 samples per cycle (s/c) are used. The impact of this factor on the protection function is mainly visualized through the time to recognize the internal fault, in Fig. 17. From this result, it can be noticed that the sampling frequency impacts on the performance, i.e., the response time is faster with higher sampling frequencies. For example, when the signal is sampled at 128 samples/cycle, the internal fault is recognized after 1,18 ms, i.e., lower than one-eight of a cycle. On the contrary, when the signal is sampled at 16 samples/cycle, the internal fault is detected only at 93,78 ms. Nevertheless, this time is lower than the traditional differential function, which provides recognition times higher than a quarter-cycle.

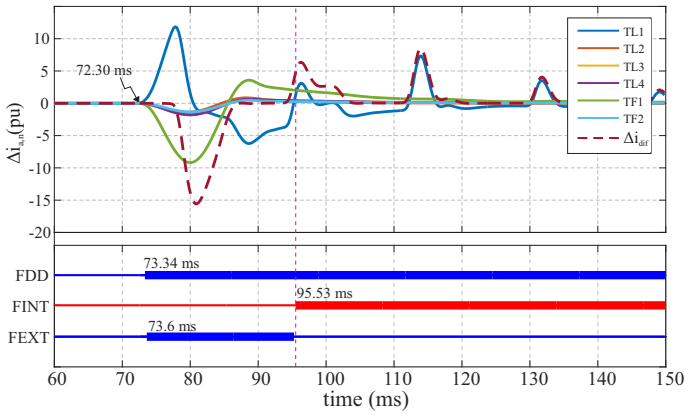

Fig. 16: Case H. One-cycle incremental quantities approach.

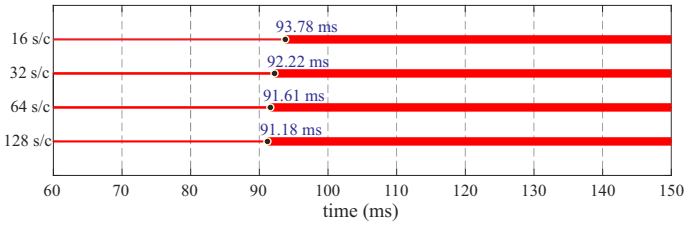

Fig. 17: Case H: Impact of sampling frequency.

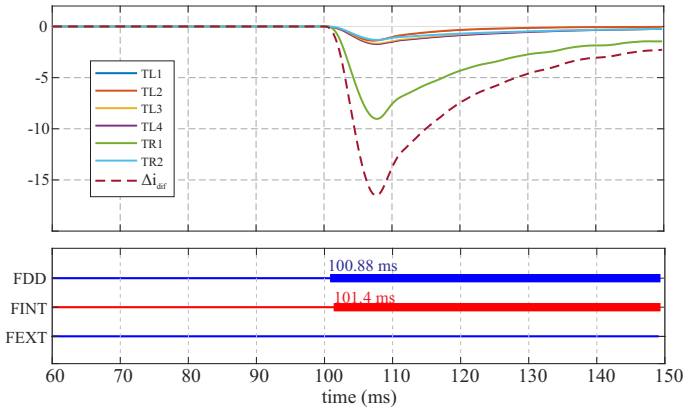

Fig. 18: Case I: Impact of noisy signals.

Thus, even though this factor impacts the response time, a low sampling frequency also provides suitable times for sending the trip command to circuit breakers in a busbar application. In addition, it can be noted that reduction of response time is less significant as sampling frequency is higher.

J. Impact of Noisy Signals

In order to test the proposed algorithm, a phase-to-ground fault, CG, is applied on Bus 2 at 100 ms. In addition, white random noise is added to the simulated signals with a signal-to-noise ratio (SNR) per sample of 40 dB. As seen in the Fig. 18, the waveforms of $\Delta i_{\phi,r}$ are not distorted and their responses are similar to previous cases where the noise was not incorporated. Thus, the trip command is issued to circuit breakers at 101,4 ms. This is because of the presence of the low-pass anti-aliasing filter used to eliminate high-frequency components. In view of that, the presence of noise does not represent a drawback for the proposed algorithm.

K. Comparison with Existing Techniques

From simulations, the mean operation time for internal fault is 1,6 ms. Between the cited papers, faster responses are found only with transient-based methods as [13], [14], [15], [23], for example. Nevertheless, critical angle faults or high resistance faults may impact the accuracy of these algorithms. As shown in Sections III-A and III-G, this is not a drawback for the proposed algorithm. On the other hand, the proposed method uses 64 samples per cycle which is a low value if compared with [10], [13], [23], [15]. The proposed function can then be implemented in cheaper devices with low sampling frequencies without considerable reduction of its accuracy and speed. Moreover, unlike [5], [17], this protective element does not need additional harmonic restraint in front of a CT saturation scenario. By the way, the proposed technique is fast because no phasor estimation of fundamental or harmonic components is necessary, but it is implemented in time domain. Also, its implementation on existing commercial relays is possible because of the simplicity of signal processing and calculations, unlike those methods that need previous training with numerous scenarios simulations as performed in [16], [17], [18]. Finally, the proposed method is segregated per phase so it is applicable to monopolar operation of circuit breakers, contrary to the algorithms proposed in [9], [20] which loss this characteristic due to the mathematical transformation used in the formulation.

IV. Conclusions

The proposed busbar protection method applies the differential and directional principles on the incremental currents. The algorithm meets the principal requirements for a busbar relaying system, once it rapidly operates when an internal fault occurs, even when there is a high fault resistance or when the fault angle is adverse. Also, it inhibits the trip command in case of an external case, even when severe CT saturation happens. The time-domain approach with the calculation of half-cycle incremental currents based on samples allows to rapidly detect evolving faults. Additionally, this technique does not consider the busbar protection zones logic for determining the differential signal, due to the use of the check zone. In that sense, the strategy for identifying a faulted bus consists of comparing the direction of the incremental currents obtained from CTs installed on the interconnection circuit with the differential incremental signal. Then, the states of switch disconnectors and circuit breakers must be known for defining the circuits to be disconnected from the faulted bus. Another configuration deserves a particular evaluation for this selection logic. Finally, it is for all of these reasons that this proposal could be a candidate for a commercial busbar protection function.

References

[1] H. J. A. Ferrer and E. O. Schweitzer., *Modern Solutions for Protection, Control and Monitoring of Electric Power Systems*. Pullman USA: Schweitzer Engineering Laboratories, Inc., 2010.

[2] *IEEE Std C37.234 - Guide for Protective Relay Applications to Power System Buses*, IEEE Power & Energy Society, Power System Relaying Committee, 2009.

[3] A. Guzman, B.-L. Qin, and C. Labuschagne, "Reliable busbar protection with advanced zone selection," *IEEE Transactions on Power Delivery*, vol. 20, no. 2, pp. 625–629, April 2005.

[4] *SEL-487B Bus Differential and Breaker Failure Relay, Instruction Manual*, Schweitzer Engineering Laboratories, Inc., Pullman, WA,USA 2018.

[5] F. A. M. Vásquez and K. M. Silva, "Instantaneous-power-based busbar numerical differential protection," *IEEE Transactions on Power Delivery*, vol. 34, no. 2, pp. 616–626, 2019.

[6] M. Hossain, I. Leevongwat, and P. Rastgoufard, "Revisions on alpha plane for enhanced sensitivity of line differential protection," *IEEE Transactions on Power Delivery*, pp. 1–1, 2018.

[7] S. Jena and B. R. Bhalja, "Numerical busbar differential protection using generalised alpha plane," *IET Generation, Transmission Distribution*, vol. 12, no. 1, pp. 227–234, 2018.

[8] R. G. Bainy and K. M. Silva, "Enhanced generalized alpha plane for numerical differential protection applications," *IEEE Transactions on Power Delivery*, pp. 1–1, 2020.

[9] S. Jena and B. Bhalja, "Sampled value-based bus zone protection scheme with dq-components," *IET Generation, Transmission & Distribution*, vol. 14, pp. 4520–4528(8), October 2020.

[10] M. Eissa, "Developing busbar protection with new differential characteristics to solve the breakpoint settings of digital commercial relays," *International Journal of Electrical Power & Energy Systems*, vol. 98, pp. 1–10, 2018.

[11] S. A. Gafoor and P. V. R. Rao, "A transient current based busbar protection scheme using wavelet transforms," *International Journal of Electrical Power & Energy Systems*, vol. 33, pp. 1049–1053, 2011.

[12] M. M. Eissa, "New differential busbar characteristic based on high frequencies extracted from faulted signal during current transformer saturation," *IET Generation, Transmission Distribution*, vol. 8, no. 4, pp. 619–628, April 2014.

[13] K. M. Silva, A. M. P. Escudero, F. V. Lopes, and F. B. Costa, "A wavelet-based busbar differential protection," *IEEE Transactions on Power Delivery*, vol. 33, no. 3, pp. 1194–1203, 2018.

[14] M. Lashgari, "Ultra-fast busbar protection employing fast s transform of current signals," *International Journal of Electrical Power & Energy Systems*, vol. 114, 2020.

[15] H. Wu, X. Dong, and Q. Wang, "A new principle for initial traveling wave active power differential busbar protection," *IEEE Access*, vol. 7, pp. 70 495–70 512, 2019.

[16] M. Gil and A. A. Abdoos, "Intelligent busbar protection scheme based on combination of support vector machine and s-transform," *IET Generation, Transmission Distribution*, vol. 11, no. 8, pp. 2056–2064, 2017.

[17] S. Jena and B. R. Bhalja, "Development of a new fault zone identification scheme for busbar using logistic regression classifier," *IET Generation, Transmission Distribution*, vol. 11, no. 1, pp. 174–184, 2017.

[18] N. G. Chothani and B. R. Bhalja, "A new algorithm for busbar fault zone identification using relevance vector machine," *Electric Power Components and Systems*, vol. 44, no. 2, pp. 193–205, January 2015.

[19] M. M. Eissa, "A novel digital directional technique for bus-bars protection," *IEEE Transactions on Power Delivery*, vol. 19, no. 4, pp. 1636–1641, Oct 2004.

[20] S. Song and G. Zou, "A novel busbar protection method based on polarity comparison of superimposed current," *IEEE Transactions on Power Delivery*, vol. 30, no. 4, pp. 1914–1922, 2015.

[21] S. P. Valsan and K. S. Swarup, "Computationally efficient wavelet-transform-based digital directional protection for busbars," *IEEE Transactions on Power Delivery*, vol. 22, no. 3, pp. 1342–1350, July 2007.

[22] S.Jena, "Initial travelling wavefront-based bus zone protection scheme," *IET Generation, Transmission & Distribution*, vol. 13, pp. 3216–3229(13), August 2019.

[23] M. Lashgari, "Fast transient-based detection of busbar faults employing improved morphological gradient," *IET Generation, Transmission & Distribution*, vol. 14, pp. 1458–1466(8), April 2020.

[24] *EMTP Reference Models for Transmission Line Relay Testing*, IEEE Power System Relaying Committee, 2004.